The Micro Technology Unlimited K-1008 Visible memory is designed to conform in most respects to the US televison standard of 525 (interlaced) lines and 30 frames per second. The exact figures with a 1.0mHz host processor are 260 non-interlaced lines and 60.096 frames per second. The European televison standard retains the same horizontal sweep frequency (15.75kHz) as the US but decreases the vertical sweep to 50Hz to match European utility power.

There is no physical reason why the vertical sweep frequency should be close to the power line frequency but there are economic reasons. CRT's are fairly sensitive to magnetic fields which manifest themselves by slightly deflecting the image if the field lines are parallel to the screen surface. AC magnetic fields from the power transformer (if the TV or monitor has one) are generally strong enough to cause about 1mm peak-to-peak deflection. If the sweep is the same frequency as the interferring field, the only effect is a slight distortion of the raster shape. If the frequencies are different, the distortion undulates through the raster causing swimming if the difference is small (.5 to 3Hz). For larger frequency differences the image appears to jitter, particularly when viewed at close range which is typical with computer displays. Even if the power transformer is adequately shielded or absent, ripple in the DC voltages used by the deflection circuits can cause variation in the raster width or height with the same swimming or jittering effect. Thus power frequency synchronous sweep allows the use of high radiation transformers and inadequately filtered unregulated power supplies without objectionable image degradation.

The standard MTU K-1008 Visible Memory gives good results with a high quality video monitor regardless of the power line frequency. All that is normally required is adjustment of the vertical hold control to lock into the 60Hz vertical sync signal. Any residual jitter can be reduced by shileding or moving the power transformer in the monitor. Ordinary sheet steel has rather poor shielding properties. Best results are obtained with special shielding foils. Laminations salvaged from a large transformer (such as a power distribution transformer) can also be formed into an effective shield. Moving the transformer away from the tube is usually easiest however. This can be accomplished by making an extension cable to the transformer, ideally with a plug and socket so the transformer can be unplugged when the monitor is moved. Where unregulated DC voltages are used in the monitor, the filter capacitors can be increased in size to reduce jitter. A value approximately 5 times the original value should eliminate jitter from this source.

The K-1008 can be coaxed into a 50Hz vertical rate simply by reducing the system clock rate from 1.0mHz to 833.33kHz. The phase locked loop on the Visible Memory will have to be adjusted to lock into the new clock rate. A disadvantage besides the 16% reduction in system speed is the reduction of horizontal sweep frequency to 13kHz. This frequency reduction results in a louder horizontal squeal and an increase in raster width. The latter can be rectified by adjusting the width coil or changing taps on the flyback transformer.

Another possibility is actual modification of the vertical freqency divider on the Visible Memory. This requires the addition of a 74LS21 IC, some etch cuts, and some jumper wires. The marked-up schematic on the next page shows the modifications and a list of instructions. With these modifications, the number of non-interlaced scan lines is increased to 312 and the vertical sweep frequency is reduced to 50.08Hz. The display format remains the same at 320 dots wide by 200 lines high however. With this simple modification the vertical sync width is greatly increased from .25MS to 3.58MS. This should not harm anything but may make the vertical sweep unstable unless the vertical hold control on the monitor is adjusted. Also the image portion of the raster may be shifted down somewhat on the screen but should still be completely visible.

50Hz Vertical Sweep Modification Instructions

___ 1. Cut trace running from U31-3 to U46-1

___ 2. Cut trace running from U31-3 to U32-2

___ 3. Cut trace running from U47-1 to U46-12

___ 4. Obtain a known good 74LS21 dual 4-input AND gate and glue it upsidedown on the top of the board between U47 and U32. Alternatively it may be mounted on a piece of perf-board mounted on the back edge of the VM board close to the video output jack.

___ 5. Run a wire from U31-1 to pin 1 on the new IC (Rember that the added IC is mounted upsidedown so the 1-7 and 8-14 pin rows will be flipped.)

___ 6. Run a wire from U32-10 to pin 2 on the new IC

___ 7. Run a wire from U32-11 to pin 4 on the new IC

___ 8. Run a wire from U32-6 to pin 5 on the new IC

___ 9. Run a wire from U46-12 to pins 13 and 12 on the new IC

___ 10. Run a wire from U45-7 to pins 10 and 9 on the new IC

___ 11. Run a wire from pin 8 on the new IC to U47-1

___ 12. Run a wire from pin 6 on the new IC to U46-1

___ 13. Run a wire from pin 6 on the new IC to U32-2

___ 14. Run a wire from U47-7 to pin 7 on the new IC

___ 15. Run a wire from U32-14 to pin 14 on the new IC

50Hz Principles of Operation

The modification outlined above replaces a 2 input AND gate with a 4 input AND gate and converts a 4 input NAND gate to a 5 input NAND gate.

In 60HZ operation U31-3 detects the coincidence of vertical retrace (part of U45) and the accumulation of 4 counts in the vertical divider. It then generates a reset signal which clears retrace and the divider. Pin 6 of the added IC simply allows the accumulation of 56 counts before reset occurs thus giving an overall divison ratio of 256+56=312 in the vertical section. Note that vertical sync is now 56 horizontal periods long.

The other half of U45 defines the 200 scan lines used to form the image. The image is started when the vertical divider reaches count 24 and is stopped when it reaches 224. In 60Hz operation there is no need to factor in vertical retrace since the divider never reaches 24 during retrace. This is no longer true with the 50Hz modification. Therefore pin 8 of the added IC factors in the retrace flip-flop state to prevent premature initiation of the image.

1. Using the Single 5 Volt 2716's in the ROM Arrays

To use the single 5 volt type 2716, you must configure one of the ROM arrays to accept 2K ROMs. This may be done following the directions given in the manual for using TMS-2716's. Next you should make adapters which will plug into the ROM sockets on the K-1012 board and will accept a single 5 volt 2716. This can be done using a 24 pin header and a 24 pin socket. These should be connected together as follows.

1. Connect all pins on the socket to the corresponding pins of the header, except for pins 19, 20, and 21.
2. Connect pin 19 of the socket to pin 20 of the header.
3. Connect pin 20 of the socket to pin 18 of the socket or header.
4. Connect pin 21 of the socket to pin 24 of the socket or header.

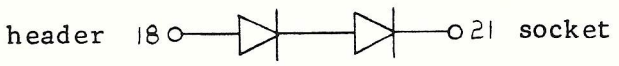
2. Programming Single 5 Volt 2716's with the K-1012 Prom I/O Board

To program single 5 volt 2716's, you must first make the following hardware modifications. The modifications given in the manual for TMS-2716's should be disregarded.

1. Cut jumper trace J4 and install jumper J5.
2. Install a wire to short out capacitor C30.

Next you must build an adapter which will plug into the programming socket on the K-1012 board and accept a single 5 volt 2716. This may also be done with a 24 pin header and a 24 pin socket. These should be connected together as follows.

1. Connect all pins of the socket to the corresponding pins on the header except for pins 18, 19, 20, and 21.
2. Connect pin 19 of the socket to pin 20 of the header.
3. Use two silicon diodes in series to connect pin 21 of the socket to pin 18 of the header as shown. (This is to drop the programming voltage from 26 volts to 25 volts.)



4. Install the adapter in the programming socket.
5. Connect pin 18 of the socket to pin 14 of U43.
6. Connect pin 20 of the socket to pin 15 of U43.

Now you must make the following changes and additions to the programming software. You should ignore the changes given in the software for TMS-2716s.

Changes

```
LINE  95  215  A9 01           LDA #1        ;ONE TIME THROUGH
LINE 100  21F  09 21           ORA #H'21     ;SET OE HIGH AND TURN VPP ON
LINE 107  231  29 DE           AND #H'DE     ;SET OE LOW AND TURN VPP OFF
LINE 190  2C8  09 10           ORA #H'10     ;SET CE HIGH
LINE 195  2D0  20 60 03        JSR DELAY50   ;WAIT 50MS
LINE 197  2D6  29 EF           AND #H'EF     ;SET CE LOW
LINE 210  2E5  4C 6B 06 LOAD   JMP NEWLOAD   ;NEW READ BYTE CODE
LINE 246  31F  69 08           ADC #H'08     ;PROGRAM 2K BYTES
LINE 265  33D  09 3F           ORA #H'3F     ;SET BITS 0-5 TO OUTPUTS
LINE 270  34A  29 E0           AND #H'E0     ;SET CE LOW, ETC.
LINE 271  24C  09 20           ORA #H'20     ;SET OE HIGH
```

ADDITIONAL CODE

```
360  A0 32     DELAY50: LDY #50     ;50MS
362  A2 C8     DLY1MS:  LDX #200    ;1MS
364  CA        LOOP:    DEX
365  D0 FD              BNE LOOP
367  88                 DEY
368  D0 F8              BNE DLY1MS
36A  60                 RTS
36B  AD 0A FE  NEWLOAD: LDA PORTBD
36E  29 DF              AND #H'DF   ;SET OE LOW
370  09 01              ORA #H'01   ;TURN ON VPP
372  8D 0A FE           STA PORTBD
375  AD 08 FE           LDA PORTAD ;READ THE BYTE
378  48                 PHA
379  AD 0A FE           LDA PORTBD
37C  29 FE              AND #H'FE   ;TURN OFF VPP
37E  8D 0A FE           STA PORTBD
381  68                 PLA
382  60                 RTS
```

Once you have saved a copy of the software, you should use the following procedure to bring up your system to perform the programming. The 2716 to be programmed should be inserted in the adapter while the system power is off. Make sure the programming voltage switch is off, i.e. away from the programming socket. This will prevent accidental programming of the 2716 on power up. Now turn the system power on. Load in the programming software and execute the NEWPRM routine once, which will initialize the software. Finally, flip the programming voltage switch on, i.e. toward the programming socket, and proceed according to steps 5, 7, 9, and 10 of the programming procedure in the manual (page 14). The programming voltage must be on in order to read as well as program the 2716's.

We can't recommend inserting and removing the 2716's with the power on. But, if you wish to do so, make sure the programming voltage is off and that pin 12 (GND) is inserted before and removed after pin 24 (+5 volts).

ADDRESSING THE K-1008 VISIBLE MEMORY ON ODD 4K BOUNDARIES

The K-1008 Visible Memory was originally designed as a memory expansion and graphic display board for the KIM-1 microcomputer. Since expansion memory in the KIM-1, for practical purposes, starts at address 2000, it was reasonable to design the address decoding circuitry of the K-1008 for addressing on 8K (or even numbered 4K) boundaries. Subsequent introduction of the SYM-1 and AIM-65 which start their expansion addresses at 1000 now makes it desirable to be able to address the Visible Memory on odd 4K boundaries such as 1000-2FFF, 3000-4FFF, etc. This application note describes modifications that can be made to the K-1008 Visible Memory to allow this. Such modifications, if properly installed, do not affect normal operation of the board and will not void the warrenty.

The modification to be described algebraically adds hex 1000 to the incoming addresses before they reach the internal Visible Memory logic. Thus after the modification is installed, the board should be jumpered for addresses hex 1000 less than the desired starting address. Thus for addressing from 1000 through 2FFF (the most common request), the VM should jumpered for addressing from 0000 to 1FFF and the modifications below installed. If it later becomes necessary to address on an even 4K boundary, moving one wire will be sufficient to restore normal operation.

MODIFICATION INSTRUCTIONS

1.__ Using an X-acto knife, cut the lines coming from the following expansion edge fingers approximately 1 CM from the edge fingers: E-P, E-R, E-S, and E-T.

2.__ Obtain a type 74LS283 four bit adder IC. Many sources of supply advertise in Byte magazine and Popular Electronics.

3.__ Spread the pins out straight horizontally and glue the 74LS283 to the back of the K-1008 right below the center of the large 1000uF 25 volt capacitor. Glue the IC right-side-up so that the normal counter-clockwise pin numbering is retained. Clip the leads if necessary to make the IC fit in the space. Silicone rubber cement or epoxy glue is recommended.

4.__ Connect the following pins of the added IC to ground (pin 7 of U3 is a good ground): __2, __6, __8, __11, and __15.

5.__ Connect the following pins of the added IC to +5 volts (pin 14 of U3 is a good source of +5 volts): __7, __16.

6.__ Add the following wires:
- __ E-P to pin 5 on added IC
- __ E-R to pin 3 on added IC
- __ E-S to pin 14 on added IC
- __ E-T to pin 12 on added IC
- __ U1-12 to pin 4 on added IC
- __ U2-5 to pin 1 on added IC
- __ U2-3 to pin 13 on added IC
- __ U2-1 to pin 10 on added IC
- __ Pin 9 on the added IC should have no connection.

7. The modification is complete. Its effect may be negated by connecting pin 7 of the added IC to ground rather than +5 and leaving the remaining connections intact. Also on SYM-1 and AIM-65 systems, U1 is not needed and may be removed to minimize address bus loading.

The Rockwell AIM-65 microcomputer is a well designed single board computer capable of considerable on-board and off-board expansion. This application note will discuss optimum usage of this expansion capability as well as a method of freeing up four 512 byte blocks of addresses in the range of A000 to AFFF for additional I/O addressing capability.

ADDING READ/WRITE MEMORY TO THE AIM-65

In the standard AIM-65, addresses from 0000 to 9FFF are available for up to 40K of contiguous RAM. The first 4K of this can be (but doesn't have to be) supplied on-board by 8 type 2114 RAM chips. The remaining 36K must be added externally through the expansion port. Some of the possible configurations of MTU products in AIM-65 systems are listed below:

1. 12K system. Expand on-board to 4K and then add a K-1008 Visible Memory addressed from 1000 to 2FFF. When using the display, 4K of memory is available. When not using the display, 12K of contiguous memory is available. Application note 5 describes how to address a Visible Memory on odd 4K boundaries.

2. 20K system. Expand on-board to 4K and then add a K-1016 16K memory board addressed from 1000-4FFF. This will give a total of 20K which is very useful for large text files, assemblies directly in memory, or large BASIC programs.

3. 28K system This is the same as the 20K system described above except that a Visible Memory has been added. Recommended addressing of the VM is from 6000-7FFF (for upgrading to disk as described below). Alternatively the VM may be addressed from 5000-6FFF (see application note 5) to give 28K of contiguous memory when the display is not being used.

4. 36K system This is the ultimate in a memory intensive system. 4K of on-board memory is used followed by two K-1016's, one addressed from 1000 to 4FFF and the other addressed from 5000-8FFF. A K-1012 ROM/IO board can provide 2708 type PROM to fill the block from 9000 to 9FFF and the I/O page can be put in the A000 block as described on the back of this sheet.

5. Disk System This represents a completely populated AIM-65 system with all addresses used and up to 4 million bytes of disk storage available. The system consists of an AIM-65 with its on-board RAM removed, a K-1016 16K memory board addressed from 0000 to 3FFF, a K-1013 disk controller with User RAM addressed from 4000-5FFF and System RAM addressed from 8000-9FFF, and a K-1008 Visible Memory addressed from 6000-7FFF. Additional I/O capability can be provided by a K-1012 ROM/IO board with its I/O page set to AF (see AIM modifications on the back of this page). When using the display, 24K of contiguous memory is available which increases to 32K when not using the display. Note that with a disk based system there is less need for the Assembler and BASIC ROM's on the AIM thus the space they use could be freed up for a Visible Memory addressed from C000 to DFFF. This would then give a clear 32K of contiguous memory even with the display in use.

OPTIMIZING USAGE OF THE AIM-65 I/O BLOCK

The AIM-65 uses an entire 4K block of addresses from A000 to AFFF to address its numerous I/O functions. Of these 4096 possible addresses, only 248 are actually "used" however. Due to the address decoding logic in the AIM, the remaining 3848 addresses map back into the 248 used ones and therefore none are left over for use by external bus interface boards. Fortunately a very simple modification to the AIM-65 computer board, which does not involve any trace cutting, can be made which will free up 2048 of these addresses in four blocks of 512 bytes each. This modification in no way affects normal AIM-65 operation or any user program that uses the published addresses of the AIM-65 I/O ports.

MODIFICATION PROCEDURE

To make the modification, follow these steps:

1. Disconnect the AIM from its keyboard and any power supplies and turn it over on its back.

2. Locate IC's Z13 and Z19 and locate their pin 1 designation.

3. Connect a jumper wire from Z13 pin 11 to Z19 pin 1. Fine guage insulated wire, such as #30 wire-wrap wire is recommended.

4. Locate Z9 which is the 6502 microprocessor chip.

5. Connect a wire from Z9 pin 18 to Z13 pins 12 and 13.

6. The modification is complete. If necessary the AIM may be restored to its original condition simply by removing the two wires.

7. Reassemble the AIM and power it up. It should operate normally.

8. Look at memory location A200. Its contents will probably read A2. Likewise A300 will show A3, A600 - A6, A700 - A7, AA00 - AA, AB00 - AB, AE00 - AE, and AF00 - AF. This proves that nothing on-board the AIM is responding to these addresses.

The modification works by enabling the address decoder for I/O addresses only when bit 9 of the address bus is a logic zero. Z13, which is a 74LS00 IC, is wired as an inverter which inverts address bit 9 so that the active-high enable input to the 74LS155 decoder, Z19, is high when A9 is low. The 4.7K pullup resistor that is connected to the decoder's enable input causes no ill effects when left in the circuit.

USAGE OF THE FREED UP SPACE

The modification listed above frees up the following blocks of memory on the AIM-65: A200-A3FF, A600-A7FF, AA00-ABFF, AE00-AFFF. The most likely usage is for the I/O page of one or two K-1012 ROM/IO boards. The first K-1012 should have its I/O page set to AE and the second K-1012 should be set for AF. Unfortunately the 512 byte blocks are not large enough for any of the PROM's on the K-1012 so PROM, if used, should be assigned elsewhere in the AIM's address space. Another use for the space would be in custom bus interface circuits constructed on a K-1020 Prototyping board.

The Qume DataTrack-8 floppy disk drive is one of the finest double-sided 8 inch floppy disk drives made. Unfortunately, it is difficult to determine the correct settings of the drive's various jumpers for proper operation with the K-1013 disk controller and CODOS operating system. This note explains the correct setting of each of the Qume disk drive jumpers.

1. Position the disk drive horizontally so that you are facing its printed circuit board and the disk door is toward your left.

2. The DRIVE SELECT jumpers can be found in the lower right corner of the board. Look for a horizontal row of 8 long, square posts sticking up and labelled DS1 DS2 DS3 DS4. For drive 0 you must connect the two adjacent posts labelled DS1 together. If you have two or more drives, you should wire the DS2 posts together instead for the second drive, DS3 for the third, etc. You may have been supplied with a black slip-on plug which makes the task of changing the drive number easier. The 4 pairs of square pads immediately below the row of 8 posts should be completely separate and not connected to anything. The 3 rows of 3 square pads each below the 4 pairs are not important.

3. On the extreme right side of the board about 2/5 up from the bottom will be found a vertical row of 8 square posts labelled 2S DC D C. The two pins labelled 2S should be connected together. The 2 pins labelled D should be connected together. The 2 pins labelled C should be connected together. The 2 pins labelled DC SHOULD NOT be connected together.

4. Immediately to the left of the vertical row of posts will be found an IC socket with a "programmable DIP shunt" plugged into it. The DIP shunt has 8 links which look somewhat like fuse links running accross it. These are labelled A B X R I Z HL and one that is not labelled. The links accross A, B, R, I, and the blank one at the left end must be intact or bridged. The links accross X, Z, and L must be cut or missing. We have found it easient to remove and discard the DIP shunt and instead use little wire jumpers similar to those used as jumpers in our boards.

5. about 2 inches from the left edge and 3 inches up from the bottom of the board are two horizontal rows of 8 square posts each. The bottom row is labelled GND HA T40. The top row is labelled GND DS DL Y. The pair of posts marked Y should be connected together. The remaining 14 posts should be free of connections.

6. Near the geometric center of the board will be found IC U3D which is a 7400. Immediately below this IC is a pair of square pads marked S. These pads are normally connected together by a printed circuit line. This connection between the two pads must be cut with a sharp knife.

7. If your system is to have 2 or more drives, remove the termination resistors on all drives except drive 0 (the one with the DS1 jumper installed, see step 2). The resistors look like IC's and are plugged into sockets immediately adjacent to the signal cable connector half-way up the right side of the board and are labelled 1TM and 2TM. If more that one drive has the termination reisitors, system operation may be intermittant.

The above instructions should be sufficient for configuring a new, standard DataTrack-8 drive. If you have purchased a used drive or have reason to believe that it has not come directly from QUME (i.e., surplus house, bankruptcy sale, etc.) check the other jumper settings described on the back of this page.

ADDITIONAL JUMPER SETTINGS

8. Just above the drive selection jumpers described in step 2 is four rows of 2 square pads each marked M, S1, S2, and S3. The row marked S2 should have a printed circuit bridge connecting the two pads. There should also be a bridge from the left S2 pad to the left S1 pad. The other two rows should not be bridged.

9. Further up is a horizontal row of 3 square pads marked L2 and L1. The rightmost 2 (marked L1) should be bridged.

10. Left of the drive selection jumpers will be found a pair of square pads marked DS. There should be no bridge between them.

11. Immediately above the DIP shunt socket will be found two square pads marked R and I. There should be no bridge between them.

12. Further up is a horizontal row of 3 square pads labelled LC and LS. There should be a bridge between the rightmost 2 pads (the pair labelled LC). The leftmost pad should be isolated.

13. Moving to the left, there is another horizontal row of 3 square pads labelled WP and NP. Again the rightmost pair (labelled WP) should be bridged.

14. Going directly down about 3/4 inch is another horizontal row of 3 square pads labelled R1 and RR. There should be a bridge accross all 3 of them.

15. About 1.5 inches down from the top and in the center of the board is a horizontal row of 3 posts (wide spacing) labelled GND 1A 1B next to a row of 8 posts (narrow spacing) labelled 2B 2A 3 4 5 +6 +12 +17. These are test points are should have no connections made to the posts.

16. At the extreme bottom left is a column of 12 square pads labelled A1 A2 A6 A7 B8 A9 B10 A11 B12 A13 B14 B15. There should not be any bridges accross any of these pads.

17. At the extreme right edge of the board next to the signal cable connection are 7 square pads. They should be connected to the edge fingers and other circuitry by PC lines but should not be connected to each other.

EFFECT OF JUMPER SETTINGS

The effect of these jumper settings is as follows:

1. READY, TRACK 0, and INDEX are daisy chained (that is, asserted only when DRIVE SELECT is true).

2. Stepper motor power is continuously applied.

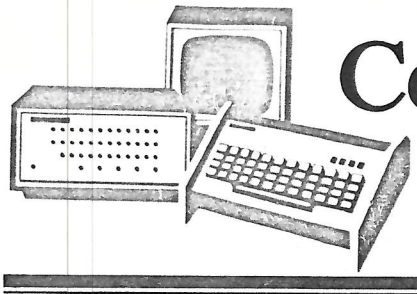
3. The head is loaded only when DRIVE SELECT and HEAD LOAD are both true.

4. The front panel activity LED lights when the head is loaded.

5. Normal double-sided operation using pin 14 to select the diskette side.

6. The circuit that inhibits READY when side 2 of a single-sided diskette is accessed is disabled (<u>required</u> for proper double-sided operation with K-1013).

PE V.15 #1 Jan. 1979



Computer Bits

By Hal Chamberlin

UPDATE ON GRAPHICS

WHEN PERSONAL microcomputers were first introduced, input/output facilities were a problem. The norm was a front panel brimming with toggle switches, and rows of binary lights representing memory and register contents. Some experimenters might have purchased a surplus Teletype for external communication with the computer system. But a "television typewriter" with 16 lines of 32 characters was considered to be sophisticated, indeed, while graphics was an unheard of luxury.

In contrast, many of the present crop of packaged and modular computers have CRT display provisions, many capable of displaying as much as 24 lines of 80 characters on the screen. Moreover, graphics capability of some kind is common today, implemented in a variety of ways, and with a wide range of capabilities.

The obvious reason for incorporating video provisions in today's breed of computers is to meet computer users' desires and needs for video. Many computer users, for instance, are interested in increasingly complex, realistic game boards; others wish to pursue creative computer art techniques. Schools form a large block of potential customers, too, with growing interest in graphics for teaching mathematics and physics concepts. Even business applications can use graphics for billing display, financial analysis, word processing, etc.

When selecting a system for a graphics application one must be careful to properly evaluate the capabilities of the systems being considered. There is a large variation in display quality, screen capacity, image resolution, image restrictions, and ease of display programming. For example, photographs of the display screen can be misleading, particularly when in color. As we shall see later, display quality depends heavily on the display monitor and the interface method utilized. Sometimes the images displayed have been painstakingly programmed a bit at a time solely for promotional reasons. Real software support for producing or working efficiently with the image shown may not be available. Also, many graphics systems have severe limitations on the types of images that can be displayed. Therefore, even if the "promotional" video example is possible, other images of similar complexity may not be.

The Display Monitor. If the system being considered does not include its own display (CRT) monitor, the user will have to provide one. The method of connecting a computer to the display is vitally important in determining the resulting image quality.

The least costly and most convenient method is via an r-f modulator connected to the antenna terminals of a television receiver. The r-f modulator simply transmits the computer's video signal on a locally unused channel, via a coaxial cable, to the TV. Unfortunately, in this approach, the display quality is mediocre at best. The sharp cutoff of video frequencies beyond about 3 MHz produced by the sound traps, cause horizontal smearing of characters and images so that 32 characters or 200 dots across is about its limit.

Even if brightness and contrast controls are carefully adjusted for an acceptable picture, the absence of dc-restoration in virtually all TV receivers causes the brightness to shift considerably as screen content changes. The result worsens with systems providing color video.

At this time the r-f modulator needed to effect this interface method is not supplied with the computer. Thus, the user must procure one. A recent FCC directive, however, emphasizes that all such modulators be type approved when combined with a computer since they fall into a Class I device category. Furthermore, the FCC has enjoined r-f modulator makers to desist in selling the devices separately!

The other—and by far preferable method of interface—is direct video to a broadband closed-circuit TV monitor. With this method, r-f modulation/demodulation distortions and the potential for external interference are bypassed. Video frequency response to 10 MHz and beyond is routine, producing sharp edges and consistent brightness to video characters and lines. Broadband monitors are expensive, however, with monochrome units costing from $150 to $300 and color starting at about $500.

Monitors usually have such features as excellent voltage regulation, improved sweep linearity, sharper CRT focus, and dc restoration. When shopping for a used surplus monitor, be sure that the model accepts *composite* video input, since some require separate horizontal, vertical, and video drive signals at TTL logic levels.

A TV receiver can also be converted to a monitor by a knowledgeable hardware person. Although a vast improvement over r-f modulation, the display is not as "clean" as with a true monitor. Usually, an isolation transformer must be added, which increases expense.

Many of the newer computers include a color-display capability. To realize the potential advantages of color, direct video into a color monitor is required. Even so, the display appearance is likely to be visibly worse than that of a monochrome display. Signal degradation is the result of NTSC encoding of the color signal necessary for composite color video. The blues and greens are limited to 1.5 MHz, while red is good only up to 500 kHz. The consequence is that 16 to 20 characters (about 100 dots) is the limit of usable color resolution. Also, unless the monitor is carefully converged, the edges of characters in corners of the screen may be a rainbow of colors, even when color is not being used. The best color systems utilize direct red-green-blue input. Generally, this is only available on a computer system with an integral CRT.

Graphic Generator Techniques. Almost every system or board that does so offers graphics capability in a different way. The wide variety of approaches used is a result of four difficult problems faced by graphics interface designers. The first is *memory usage*, since the image on the screen must be encoded into bytes stored in memory. The second is the amount of graphic detail or *resolution* that it is possible to display. The third is *flexibility*, or the variety of image types

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that can be displayed. And the fourth is *compatibility* with character generators so that nongraphics applications are simplified.

These are conflicting requirements. For example, a high-resolution flexible display will require considerable memory to store the image. On the other hand, maintaining compatibility with character generators minimizes memory usage but limits resolution and flexibility.

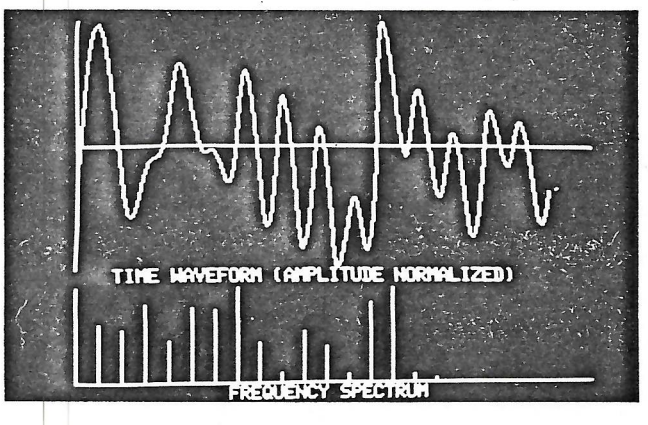
In most cases, designers have opted for compatibility with character-oriented displays. Such a display divides the screen into rows and columns of *character cells*. The PET computer for example, uses 25 rows of 40 characters per row for a total of 1000 character cells. Each cell, in turn, is divided into *pixels* or dots; the PET uses 8 rows of 8 dots per row. The characters that make up the display are therefore displayed centered in the character cells and are, in turn, composed of the dots. Each byte of display in the PET memory corresponds to a character cell. Hence, 1000 bytes (1 KB) of memory are used for the display.

Graphic images can be formed from a special *graphics character set* used in addition to the normal ASCII character set. Shapes such as horizontal, vertical, diagonal, and curved lines are provided and can be pieced together to form crude line drawings. Special symbols, such as hearts, clubs, spades, etc., are also included for a total of 64 graphics characters. Add the 64-character uppercase ASCII subset and a bit for inverse video (black-on-white) and all 256 possible character codes are used up.

Such a display is very adept at putting on-screen gameboards, simple line drawings, and, of course, text. On the other hand, mathematical curve plotting resolution is no better than the typical character plot with "*" for points. Although one may be able to hand-fit a curve with the line segments and other shapes available, there is no software support available to do this. Moving images can also be programmed, but the movement is quite choppy since it must be in character cell increments.

A related technique employs a *programmable* character generator, such as one made by Objective Design for S-100 bus compatible display interface boards. Essentially, the usual ROM character generator is replaced by a small RAM that can be written into to provide a changeable character set. In the Sorcerer from Exidy, for example, the character to be displayed can be determined by software. Thus, it is now possible for a user to tailor the graphic character set to match the application. If the application is line drawing, the RAM can be filled with a greater variety of line segments and curves. If it is chess, chesspiece symbols can be written. Whatever graphic set is chosen, it must be used for the entire display. Even with the added flexibility, the limitations of this scheme are basically the same as with the fixed-graphic character set.

Another variation attempts to increase the screen resolution for random-dot graphics such as required for curve plotting. Radio Shack's Model TRS-80 display, for example, uses 16 rows of 64 character cells per row with a character cell being 12 rows of 8 dots each. For graphics, each character cell is divided into a two-wide by three-high array of blocks or pixels and any possible on/off combination of the six blocks can be specified. In the graphics mode, therefore, the screen becomes an array of 48 rows of 128 *blocks* per row and any conceivable combination of blocks can be on and off. While the resolution for line drawing and game boards is inferior to the graphic character generator approach, arbitrary curves are displayed with about twice as much resolution. Display memory in the TRS-80 is only 7 bits wide and comprises 1024 bytes. Normal ASCII characters take up 64 of the codes, while the other 64 codes are used to specify the 64 possible combinations of graphic blocks in a character cell.



The Micro Technology Unlimited Visible Memory in action.

Bit-Mapped Displays. An entirely different approach to graphics ignores character generators altogether and simply divides the screen up into a very large number of individual dots, with one bit of display memory for each dot. Such displays are called *pixel* or *bit-mapped* displays to distinguish them from character displays. If a sufficient number of dots are provided, this is by far the most flexible graphic display technique because there are no restrictions on image type or placement.

When using the proper software, even text can be displayed with complete freedom as to character shape, size, and placement. This makes possible bold headlines, tilted italics, subscript and superscript for math and chemical equations, and proportionally spaced text for clean right-margin justification. Their main disadvantage is that a large amount of memory is needed for a high resolution display. Upwards of 8K bytes is not uncommon.

The Apple II computer, for example, has a black-and-white pixel display mode with 192 rows of 240 dots per row which is sufficient resolution for well detailed drawings, graphs, and charts. The 120 by 96 full-color mode, which can display 7 colors at two intensity levels and black, is less useful for curve plotting but is capable of beautiful computer art.

Users of KIM-1s can use the Visible Memory (see photo), which provides a 320-wide by 200-high dot matrix as well as 8K of refresh memory, all on one board. Owners of S-100 bus micros can utilize a new graphics interface from Vector Graphics that provides a 256 by 240 image in black and white or a 128 by 120 image with 16 levels of gray. The latter mode is useful for half-tone picture processing and display in applications such as amateur slow-scan TV.

Software support is important in any graphics application, particularly if one BASIC is used. Although the user can perform any graphic operation by POKEing data into memory, BASIC is likely to be very slow in manipulating the large amount of data required. Radio Shack, on the other hand, provides BASIC statements for setting and resetting any graphic cell given its *X* and *Y* coordinates. The Apple provides statements for setting the coordinates of endpoints and will automatically and rapidly draw the best straight line connecting them.